## REMARKS

Claims 1 to 4, 7 to 19, and 21 to 29 are pending, of which claims 1, 12, 14 and 26 are independent. Favorable reconsideration and further examination are respectfully requested.

Independent claims 1, 12 and 26 were rejected over U.S. Patent No. 6,274,937 (Ahn) in view of U.S. Patent No. 6,628,178 (Uchikoba), U.S. Patent No 6,091,310 (Utsumi), and newly-discovered U.S. Patent Publication No. 2003/0107056 (Chin). Independent claim 14 was rejected over Ahn, Uchikoba, Utsumi, and Chin in view of U.S. Patent No. 6,060,954 (Liu). The rejections of the dependent claims include rejections over the primary references and previously-cited Chakravorty, Li, Asahi, Figueroa, Daniels, and Juskey.

With respect to claim 1, as explained in the response filed on June 4, 2009, the Examiner interprets the claim term "symmetrical signal" as follows:

> wherein at least one input and/or at least one output of the at least one chip component [120] conducts a symmetrical signal [electrically conductive materials are capable of conducting symmetrical signals such as sine waves, saw waves, square waves, etc.]. [1]

As used in this application, a symmetrical signal is one of two signals that propagates along symmetrical signal lines, not a single signal.[2] We do not understand this to be disclosed in Ahn.

In response, an Advisory Action issued which states the following:

[1] Office Action, page 3
[2] See, e.g., page 10, lines 18 to 22 of the English-language specification

> Further, for claim 26, the claim language states, "conducts a symmetrical signal", which is shown by Ahn, since RF or radio frequency devices are used [column 1, lines 60-67], it is noted that radio frequency devices are signal transmission and receiving devices, they utilize signals and circuitry that output and receive carrier frequencies / signals, which are constant frequency signals, which are necessarily and by definition "symmetrical signals".

In this regard, we note that merely referencing an RF device is not sufficient to render obvious use of symmetric signals in inputs or outputs thereof. More specifically, RF systems may employ asymmetric signals for transmission. As we understand it, in such systems, an RF signal port includes two terminals. One of these terminals transmits "the signal" and, therefore, is labeled a "hot" terminal. The other terminal may be connected to ground. As a consequence, all signal information is provided by the hot terminal only. The ground terminal is for reference. This method of signal conduction is also called "single ended", "non-symmetric" or "unbalanced", and is understood to be well-known in the art.

By contrast, as we also understand is well known in the art, a symmetrical signal (also referred to as a "symmetric" or a "balanced" signal) includes two components, which are applied to corresponding terminals by corresponding signal lines. Both signal components are "hot" in that both transmit signal information. The phases of the signal components at the two terminals typically differ, e.g., by 180°. The amplitude of the signal components is typically equal at both terminals. A symmetric signal may be advantageous in that signal information may be taken from one, or both, terminals. Also advantageous is that influence on the signal line effecting a common mode disturbance can be balanced out by using both terminals.

We are filing an IDS herewith, which includes references that, we believe, show that one of ordinary skill in the art would understand that a "symmetrical signal" includes a signal having two components that are out-of-phase from each other.

Keeping the foregoing in mind, claim 1 now recites:

> wherein at least one of the inputs or the outputs of the at least one chip component are for conducting a symmetrical signal.

By specifying that one of "the inputs" or "the outputs" conducts the symmetrical signal, we are making clear that the signal is conducted via more than one input or output, e.g., one input may conduct one component of the symmetrical signal and another input may conduct another, out-of-phase, component of the symmetrical signal..

The applied art, including Ahn, is not understood to disclose or to suggest the use of symmetrical signals. As stated above, in the following excerpt, the March 4, 2009 Office Action appears to misconstrue the term "symmetrical signal":

> wherein at least one input and/or at least one output of the at least one chip component [120] conducts a symmetrical signal [electrically conductive materials are capable of conducting symmetrical signals such as sine waves, saw waves, square waves, etc.]. [3]

While a sine wave, a saw wave, or a square wave may be a component of a symmetrical signal, there is no disclosure in the art of the symmetrical signal that is claimed, namely, a signal conducted via two terminals, e.g., having two out-of-phase components, each of which includes signal information.

Also, in the Office Action, Chin was cited for its alleged disclosure of impedance conversion in the range claimed, namely, 5 % to 400%.

In our June 4, 2009 response, we argued that it is our understanding the Chin involves matching impedances of a printed circuit board's landing pad and trace, "thereby substantially

[3] Office Action, page 3

avoiding impedance discontinuity between the pad and the trace".[4] This may be done by adding metal strips (capacitance) to board's metal layer or reference plane, as shown in Fig. 2a. Accordingly, contrary to what is said in the Office Action, we do not understand Chin to describe an integrated impedance converter configured to transform an impedance of the at least one chip component by 5 % to 400%, but rather a method of matching impedances of elements of a printed circuit board, and matching those impedances to within 10% of each other.

The Advisory Action, however, states

> In response to the arguments on page 1 of the remarks, it is asserted that the prior art combination and specifically Chin does not show, "the at least one impedance converter is configured to transform an impedance of the at least one chip component by 5% to 400%", it is held that this argument is incorrect.
>
> It is noted that "impedance matching" means to convert an outside and incoming signal impedance to an inside signal impedance level, so as Chin states, impedance matching components effects an over 10 percent change
>
> In response to applicant's arguments on page 2 of the remarks, against the Chin reference individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The combination of Ahn in view of Uchikoba in view of Utsumi already show the particular impedance converting passive elements as claimed, just not the explicit quoted performance values. Chin is merely used to show that impedance converters in general, commonly perform at the quoted values in the claim limitations.

In response, we note that the Examiner's definition of impedance matching does not necessarily disclose or suggest transforming an impedance of the at least one chip component by 5% to 400%. For example, if the impedance of one component is 100Ω and the impedance of another component is 112Ω, to match the impedances to within 10% would only require an impedance conversion of about 2% to 3%. Consequently, while Chin may describe impedance transformation, it is not understood to render claim 1 obvious.

Regarding the comment about rebutting Chin individually, we note that page 5 of the Office Action makes clear that Chin is the only reference being relied upon for disclosure of impedance transformation by 5 % to 400%. Therefore, once it is shown that Chin does not

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[4] Paragraph 0009

disclose or suggest such transformation, there would seemingly be no need to address the remaining references, particularly in view of the following statement:

> Ahn/Uchikoba/Utsumi do not show the specifics wherein the at least one integrated impedance converter is configured to transform an impedance of the at least one chip component by 5% to 400%.[5]

For at least the foregoing reasons, independent claim 1, along with independent claims 12, 14, and 26, are believed to be patentable over the applied art.

Dependent claims are believed to define patentable features. Each dependent claim partakes of the novelty of its corresponding independent claim, in light of the foregoing amendments, and, as such, has not been discussed specifically herein.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, we respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

[5] Office Action, page 5

Please charge any fees or credit any overpayment, to deposit account 06-1050, referencing Attorney Docket No. 14219-075US1.

The undersigned attorney can be reached at the address shown above. Telephone calls regarding this application should be directed to 617-521-7896.

Respectfully submitted,

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